REMARKS

In the Office Action, the examiner objected to the drawings on the ground that Figures 1 and 2a lack prior art legends. Accordingly, the applicant has submitted concurrently herewith a request for approval of drawing changes in which a "Prior Art" label is added to Figures 1 and 2a. Replacement sheets of Figures 1 and 2a are also enclosed.

The examiner objected to Claims 5 and 6 because of the informalities where the sentences therein are incomplete. Accordingly, the applicant has amended the descriptions in Claims 5 and 6 to correct the informalities.

In the Office Action, the examiner rejected Claims 1, 7 and 8 under 35 U.S. C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. It is stated that there is no limitation as to how the test pattern is generated in the claims. Accordingly, the applicant has amended the claims to include the limitation regarding the generation of the test pattern.

With respect to the latter part of the rejection under 35 U.S.C. 112, second paragraph, regarding how the test patterns will be generated when the memory under test has different row and column sizes or when the left and right hand sides of the equation do not match with one another, it appears that the examiner misunderstands the operation of the pattern generator. The test pattern for memory testing are generated by the pattern generator

of Figure 2A. The test pattern incudes address data, control data and write data. Regardless of the row and column sizes or mismatch of the equation, the test pattern is generated by simply changing the address data for sequentially accessing the memory cells while providing the same write data such as "1". The inversion request signal of the present invention is used to invert the write data (from "1" to "0" for example) for only the predetermined memory cells accessed by the address data. In other words, the operation for generating the test pattern is not affected by difference of the row and column sizes of the memory device under test or the mismatch of the right and left sides of the equation.

The examiner rejected Claims 1-4 and 7-8 under 35 U.S.C. 102(e) as being anticipated by Nakamura (U.S. Patent No. 6,523,135). Accordingly, the applicant has amended the claims to more clearly differentiate the present invention from the teaching of the cited Nakamura reference. In the amendment, the applicant has clarified that the inversion request signals are generated for locations of specified memory cells on a diagonal line on an array of memory cells where overall numbers of memory cells in a row (X) direction and a column (Y) direction are different from each other.

The cited Nakamura reference shows the conventional technology that is also described in the background section of the present application. In the conventional technology, the operation for generating inversion request signals is successfully performed for the case where the memory device under test has the same total

number of memory cells in the row (X) and column (Y) direction, such as 4 by 4. As explained in detail with reference to Figure 6 of the present application, the conventional technology is not able to correctly generate the inversion request signals when overall numbers of memory cells in the row (X) direction and in the column (Y) direction are different from each other, such as 8 by 4 (see example of Figure 6). It is apparent that the cited Nakamura reference teaches only the case where the total numbers of memory cells in the row (X) and column (Y) directions are the same. For example, in the cited Nakamura reference, the description at column 3, lines 46-56, reads as follows:

> In the DRAM 17, the memory cell located on i-th row and j-th column (i=1,2,3,...n, and j=1,2,3,...n) is represented by Cij, wherein the DRAM 17 has a memory cell array which includes n x n memory cells. In this case, the number "N" of memory cells is $N=n^2$. The access order of all the memory cells is based on the order of C_{11}, C_{21}, C_{31},..., C_{n1}, C_{12}, C_{22}, C_{32},...., C_{n2},...., C_{1n}, C_{2n}, C_{3n},...C_{nn}, and p-th memory cell in this order is represented by C.sub.p wherein p=0, 1, 2,...N-1. In the product test, the addresses are determined in the ascending order or a descending order of "p" in the memory cell Cp.

As stated in this extract, since both the row and column have memory cells of 1 to n (i.e., n by n), there is no difference in the total number of memory cells between the row (X) and column (Y) directions. Thus, the cited Nakamura reference does not show the essential feature of the present invention in which the inversion request signal can be generated for the memory device having the different total numbers of memory cell between the row (X) and column (Y) directions.

Further, as defined in Claims 1, 7 and 8, as amended, the pattern generator of the present invention generates the test pattern including the address data, write data and control data. The cited Nakamura reference does not show this feature either. Since the essential feature of the present invention is not shown in the cited Nakamura reference, the rejection under 35 U.S.C. 102(e) is no longer applicable to the present invention.

The examiner rejected Claims 1-8 under 35 U.S.C. 102(e) as being anticipated by Ohsawa (U.S. Patent No. 6,523,135). Accordingly, the applicant has amended the claims to more clearly differentiate the present invention from the teaching of the cited Nakamura reference. In the amendment, the applicant has clarified that the inversion request signals are generated for locations of specified memory cells on a diagonal line on an array of memory cells where overall numbers of memory cells in a row (X) direction and a column (Y) direction are different from each other.

The cited Ohsawa reference shows the conventional technology that is also described in the background section of the invention where the operation for generating inversion request signals is successfully performed for the case where the memory device under test has the same total number of memory cells in the row (X) and column (Y) directions. As explained in detail with reference to Figure 6 of the present application, the conventional technology is not able to correctly generate the inversion request signals when the overall numbers of memory cells in the row (X) and in the

column (Y) are different from each other. It is apparent that the cited Ohsawa reference teaches the data inversion only for the case where the total number of memory cells in the row (X) and column (Y) direction because of the illustration of Figure 6 and the description at column 3, lines 24-36, which reads as follows:

> FIG. 6 shows a concept of generating such specific test patterns through the data inversion process. The example of FIG. 6 shows the case where a checkerboard pattern is generated for a memory under test having 16 memory cells with an X address of 4 and a Y address of 4. An example of checkerboard pattern is shown in the upper part of FIG. 6. The data generator 321 generates the data pattern shown in the upper left of FIG. 6. The address function generator 322 generates the inversion information as shown in the lower left of FIG. 6. The inversion information is indicated by one bit signal which shows "1" for each even address and "0" for each odd address.

As stated above, since the row and column have four (4) memory cells (i.e., 4 by 4), there is no difference in the total number of memory cells between the row (X) and column (Y) direction. Thus, the cited Ohsawa reference does not show the essential feature of the present invention in which the inversion request signal can be generated for the memory having the different total numbers of memory cell between the row and column directions. Since the essential feature of the present invention is not shown in the cited Ohsawa reference, the rejection under 35 U.S.C. 102(e) is no longer applicable to the present invention.

As discussed above, none of the cited references show the essential feature of the present invention where the inversion request signal can be generated for the memory having the different total numbers of memory cell between the row and column directions.

Accordingly, the applicant believes that the rejections under 35 U.S.C. 102(e) are no longer applicable to the present application.

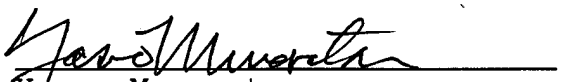
In this opportunity, the applicant has amended the specification to correct the minor errors therein and to more clearly disclose the present invention. This is to verify that no new matter has been introduced by this amendment.

In view of the foregoing, the applicant believes that Claims 1-8 are in condition for allowance, and accordingly, Applicant respectfully requests that the present application be allowed and passed to issue.

Respectfully submitted,

MURAMATSU & ASSOCIATES

Dated: 9/8/04

By: 

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IN THE DRAWINGS:

The applicant has submitted concurrently herewith a request for approval of drawing changes in which a "Prior Art" label is added to Figures 1 and 2a to overcome the objection to the drawings by the examiner.

FIG. 1 (Prior Art)

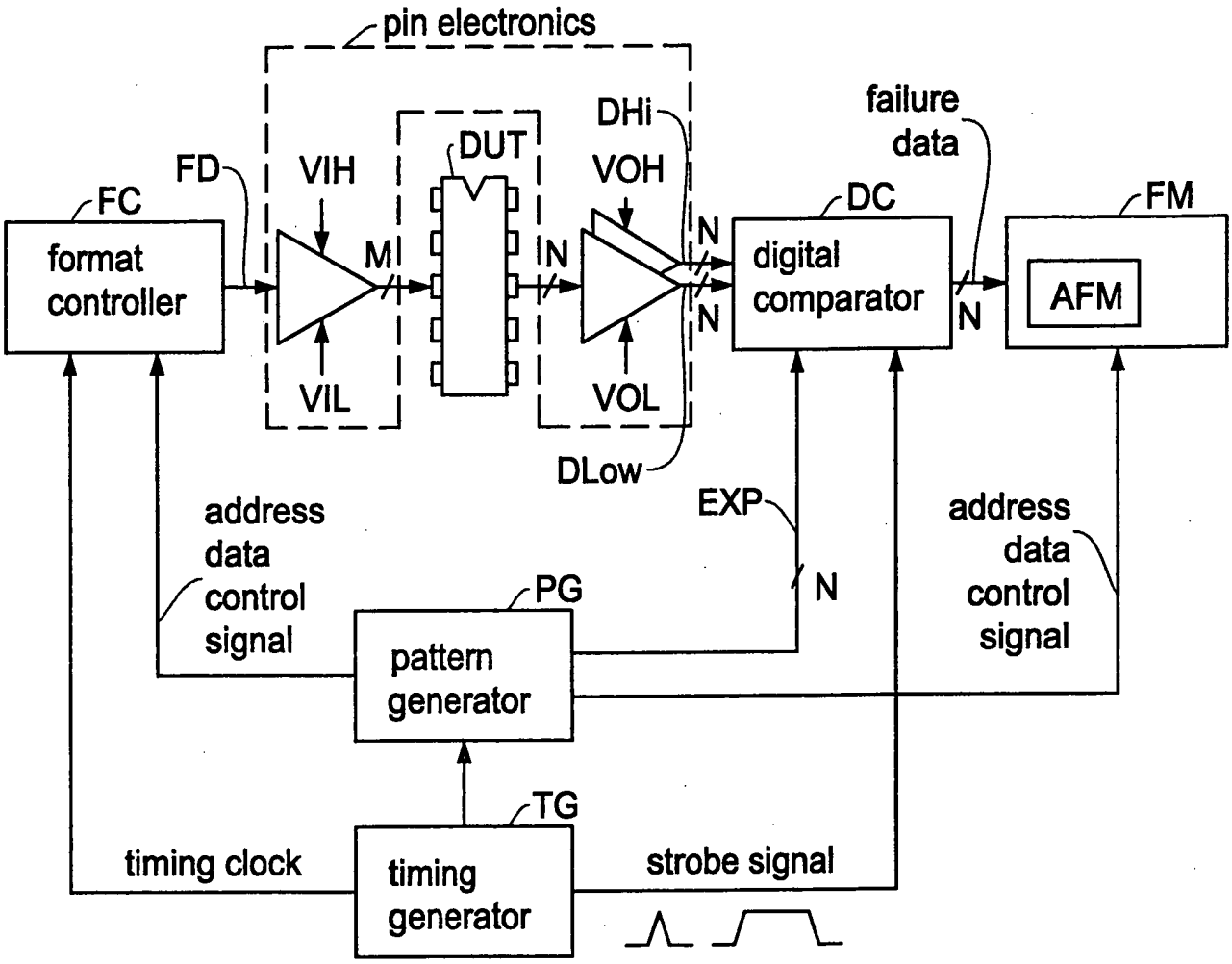

FIG. 2A (Prior Art)

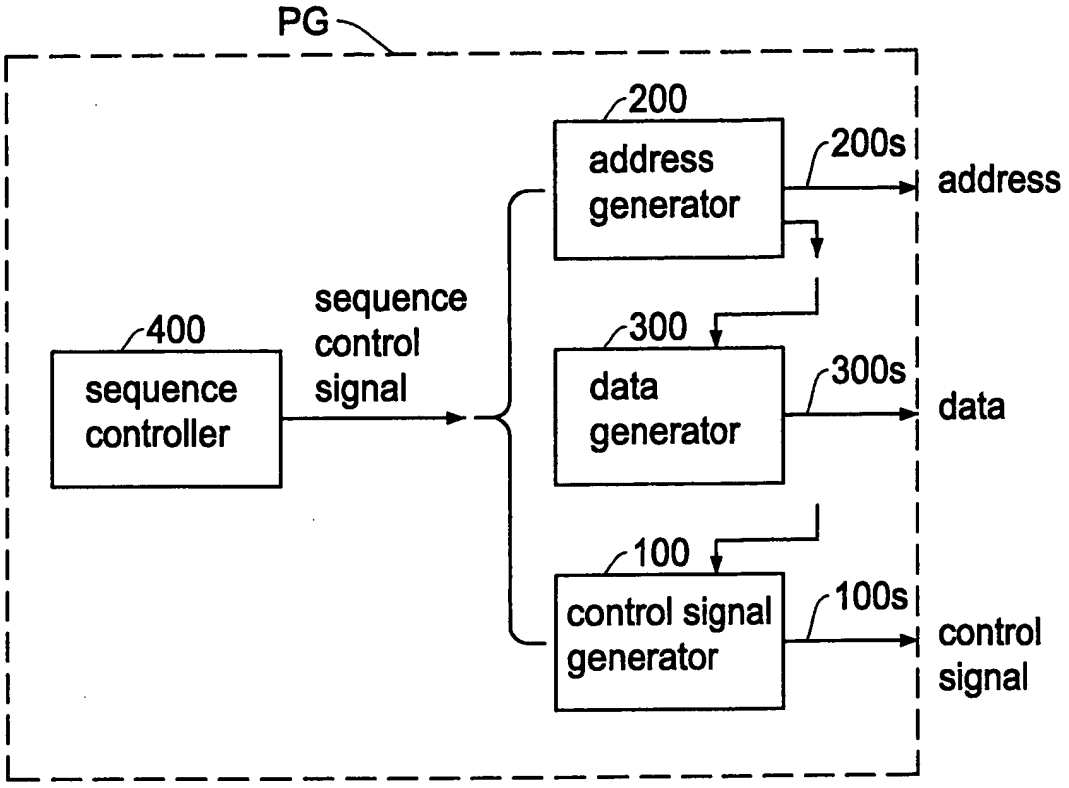

FIG. 2B